REMARKS/ARGUMENTS

Examiner Nema O. Berezny is thanked for thoroughly reviewing the subject. All claims are believed to be in condition for allowance.

Claim rejections - 35 U.S.C. § 103

Reconsideration of the rejection of claims 1-25 and 27-30 under 35 U.S.C 103(a) as being unpatentable over Dass et al. (US Patent 6,143,668) in view of Fu et al. (US Patent (5,807,787) is respectfully requested based on the following.

Dass et al. starts with a surface over which a bonding pad is provided. No pattern of metal interconnect lines has been created over the substrate used by Dass et al. The claimed invention starts with, as clearly highlighted in Fig. 8 of the claimed invention, with a bond pad 14 and patterned layers 12 of interconnect metal. The patterned layers 12 of interconnect metal are **not provided** by Dass et al., which is of critical importance to the claimed invention as stated and explained in detail in the specification of the claimed invention.

Where Dass et al. refers to interconnect lines, as kindly cited by Examiner, Dass et al. discusses prior art in which a complete package is considered. More specifically, Dass et al., col. 1 lines 26-29, cites metal interconnect lines and components of an integrated circuit device 11, wherein bond pads 13 are located along a periphery of integrated circuit device 11. In the center of the integrated device 11 is the active region 12 containing the majority of the high-density, active circuitry of integrated circuit device 11.

The top view shown in Fig. 1 of the Dass et al. invention clearly demonstrates that the bond pads 13 as not located intermixed with interconnect lines but are arranged, as cited "along a periphery" of an IC device.

The invention addresses a surface over which interconnect lines are created that are adjacent to a bond pad, allowing the creation of an opening to the bond pad while adjacent layers of interconnect are protected from etching effects.

Dass et al. therefore does not provide for the problem of surface damage to the passivation layer of interconnecting metal

lines. Dass et al. does not address the occurrence of keyholes between closely spaced layers of interconnect metal.

Applicant has, in order to further assure that the Fu et al. invention does not address the formation of keyholes as an aspect of creating interconnect metal over a semiconductor surface, again carefully reviewed the Fu et al. invention for the mentioning of the term "keyhole" therein and has, contrary to Examiner's assertions, been unable to identify this term in the Fu et al. invention ad the description thereof, thereby paying specific attention to pages 3 and 4 of the Fu et al. invention, since these pages are referred to by Examiner.

The claimed invention by contrast:

- starts with the surface of a semiconductor substrate 10, over which a pattern of metal has been created, including interconnect lines 12 and bonding pads 14
- a first (16) and second layer (18) of passivation are consecutively deposited
- a thick layer 36 of polyimide is deposited over the surface of the second layer 18 of passivation

- the thick layer 36 of polyimide is patterned and etched creating openings 38/40 in the layer 36 overlying the surface of the bonding pads 14, leaving the polyimide 36 in place above the interconnect line pattern 12,
- the layers 40/42 of passivation are etched, exposing the surface of the bonding pads 14, and
- the thick layer 48 of polyimide is cured and cross-linked in order to provide improved protection for the interconnect metal 12.

Since Dass et al. does not provide for a thick layer of polyimide overlying interconnect traces Dass et al. also does not provide for protection of the passivation film (by the thick layer of polyimide) that remains in place above the interconnecting lines.

The method that is provided by Dass et al. addresses problems that are experienced with a passive scrub cantilever needle probe card and the scrubbing process. These problems become particularly severe for smaller contact pad pitch of contact pads that are used for testing or probing of wafers. The pads

that are therefore created by Dass et al. are wafer contact pads for testing purposes having a pitch of 80 microns.

Applicant respectfully points out that, although the concept of "smaller contact pad pitch of contact pads that are used for testing or probing of wafers" is cited supra by Applicant and relating to the Dass et al. invention, this aspect of the Dass et al. invention has been discussed in order to further highlight the differences between the claimed invention and the Dass et al. invention This citation however does not imply or require that the claimed invention should specify a parameter of pitch, as suggested by Examiner, since the claimed invention for its preferred implementation is not dependent on considerations of pitch between for instance patterned traces of interconnect metal and/or a there-with associated contact pad.

Fu et al. addresses only bond pads, the instant invention addresses bonding pads that are provided on the surface of a substrate concurrent with interconnect lines.

The difference between Fu et al. and the claimed invention is significant since, in forming a thick layer of passivation (for

improved protection of the underlying components) in the era of sub-micron devices and the therewith used closely spaced interconnect lines, keyholes between interconnect lines are a problem since the thick layer of passivation (typically deposited by depositing two layers of passivation) does not readily penetrate between narrowly spaced adjacent interconnect lines.

For a typical process of etching (a passivation layer in order to expose a bonding pad) photoresist is used which, where keyholes are present, which is typically between adjacent interconnect traces, penetrates the keyholes.

During subsequent high temperature processing, the photoresist deposits violently react to the high temperatures and "explodes" from the keyholes, causing significant disturbance to the process of device formation.

This latter phenomenon is to be prevented, the present claimed invention prevents this by using a thick layer of polyimide, whereby the polyimide readily penetrates any keyholes

that may have formed between adjacent, closely spaced interconnect lines.

With the claimed invention, bond pads can be created without incurring processing damage caused by photoresist remnants that in conventional processing penetrates into keyholes between closely spaced interconnect lines.

Fu et al. deposits a layer of passivation and etches this layer, thereby exposing the surface of the bonding pad, before depositing a layer of polyimide.

The instant invention deposits the (two layers of) passivation over which the layer of polyimide is deposited. After these layers have been deposited, the polyimide is etched after which the layer of passivation is etched.

This difference in sequence between the claimed invention and the Fu invention is significant because the claimed invention first provides protection to the interconnect lines after which a bonding pad is created. Fu et al. creates a bonding pad by first creating an opening in the layer of passivation, thereby

exposing the bonding pad, after which a layer of polyimide is deposited.

Dass et al. does provide for a sequence of depositing a passivation layer, then depositing a layer of polyimide, then etching the polyimide and then etching the passivation layers.

The latter layer of polyimide, as provided by Fu, contacts the surface of the bonding pad, the layer of polyimide is etched again, thereby exposing the bonding pad. The etch of the polyimide leaves polyimide in place over the surface of the bonding pad (Fu et al., col. 6, line 1 e.a.) which is further removed with the additional step of oxide ashing (Fu et al, see table in col. 6, lines 6-14).

What makes the instant invention unique and therefore patentable over Dass et al. in view of Fu et al. is that neither one of these two inventions addresses the creation of a bond pad that has been provided over a semiconductor surface over which a network of interconnect traces has also has been provided, the interconnect traces being interspersed with the bond pad that is provided by the claimed invention. No requirement or assumption

of location of the interconnect traces with respect to the bond pad is therefore in force for the claimed invention.

The bond pad can be accessed (exposed) using methods of the claimed invention, leaving the interconnect traces covered and protected.

Prior art processing required, in order to achieve this objective, the application of layers of photoresist with the potential of forming deposits of photoresist in keyholes between adjacent layers of interconnect traces, leading to the (potentially catastrophic) results that have been highlighted above.

The claimed invention eliminates negative effects previously created in exposing a bond pad, pad 14, Fig. 9 of the invention, which is created on a surface over which also interconnect traces, lines 12, Fig. 9, have been created, as further specified in claims 1 and 20 of the invention.

Applicant respectfully disagrees with Examiner's statement that the features upon which applicant relies (i.e. the sequence

of steps, and the creation of a bond pad over a semiconductor surface in which a network of interconnect traces has been provided) are not recited in the rejected claim(s).

Applicant quotes claim 1, which specifies the method of the claimed invention for forming bonding pads of a semiconductor substrate and underlines in this quote the specific features upon which applicant relies and which are at this time part of the quoted claim 1, as follow:

- providing top level interconnecting metal for interconnecting lines and top level bond pad metal for bond pads, said top level metal being formed selectively on an insulating film overlying the main surface of a semiconductor substrate in which a desired circuit element is being formed, the surface of said insulating film being partially exposed
- depositing a passivation layer over said top-level metal and over the partially exposed surface of said insulating layer, said passivation layer comprising a first and a second passivation layer
- depositing a layer of photosensitive polyimide over said passivation layer, filling keyholes between closely spaced interconnect lines, preventing etching damage and damage of

cracking and delamination to the surface of said passivation layer, further providing a stress buffer to said passivation layer, reducing stress impact on the passivation layer

- patterning and etching said layer of photosensitive polyimide thereby forming a pattern for said bonding pads
- patterning and etching said passivation layer thereby exposing said bond pad, said patterning and etching of said passivation layer to take place after said patterning and etching of said layer of photosensitive polyimide, and
- curing and cross-linking said photosensitive polyimide said curing and cross-linking of said photosensitive polyimide to take place after said patterning and etching of said passivation layer.

Applicant argues that the sequence of the specified steps of:

- depositing a passivation layer over said top-level metal and over the partially exposed surface of said insulating layer, said passivation layer comprising a first and a second passivation layer
- depositing a layer of photosensitive polyimide over said passivation layer, filling keyholes between closely spaced interconnect lines, preventing etching damage and damage of

cracking and delamination to the surface of said passivation layer, further providing a stress buffer to said passivation layer, reducing stress impact on the passivation layer

- patterning and etching said layer of photosensitive polyimide thereby forming a pattern for said bonding pads can only be performed in the sequence in which these steps are listed since each following step depends on the (completion of) the preceding step. For instance, "depositing a layer of photosensitive polyimide over said passivation layer" can only be performed if a passivation layer is present, in other words after completion of the specified preceding clause of "depositing a passivation layer", etc.

It is therefore argued that the sequence of steps in which Applicant relies is clearly and unambiguously defined while the presence of top level interconnecting metal for interconnecting lines and top level bond pad metal for bond pads is also defined in claim 1. The creation of top level interconnecting metal for interconnecting lines and top level bond pad metal for bond pads, as suggested by Examiner, is not part of the claimed invention and therefore is not specified in the claims of the invention, just like for instance the creation of a "semiconductor substrate in which a desired circuit element is

being formed" is not part of the claimed invention and is therefore not further specified.

The claims highlighted by Examiner, such as claims 2, 21, 3, 22, 18, and the like, are dependent claims to independent claims 1 and 20. Since these claims are dependent claims to independent claims 1 and 20, and since independent claims 1 and 20 are, as argued supra, patentable over Dass et al. in view of Fu et al., Application additionally asserts that these dependent claims also may not be rejected over Dass et al. in view of Fu et al. for reasons cited by Examiner. These dependent claims specify preferred methods and conditions of the implementation of the claimed invention. Without these claims therefore the claimed invention would be open to arbitrary implementation, resulting in a deficient definition of the claimed invention such that one skilled in the art can implement the claimed invention based on the specification and the claims of the invention.

The following comments apply relative to the Dass et al. invention in view of the Fu invention, comparing these inventions with the claimed invention:

- Dass et al. starts with a surface over which a bonding pad (only) is provided

- no pattern of metal interconnect lines has been created over the substrate used by Dass et al.
- the claimed invention starts with a bond pad 14 and patterned layers 12 of interconnect metal. The patterned layers 12 of interconnect metal are **not provided** by Dass et al., which is of critical importance to the claimed invention as stated and explained in detail in the specification of the claimed invention
- Dass et al. cites metal interconnect lines and components of an integrated circuit device 11, wherein bond pads 13 are located along a periphery of integrated circuit device 11. In the center of the integrated device 11 is the active region 12 containing the majority of the high-density, active circuitry of integrated circuit device 11
- the invention addresses a surface over which interconnect lines are created that are adjacent to a bond pad, allowing the creation of an opening to the bond pad while adjacent layers of interconnect are protected from etching effects
- Dass et al. does not provide for the problem of surface damage to the passivation layer of interconnecting metal lines

- neither Dass et al. nor Fu et al. address the potential negative effects caused by the occurrence of keyholes between closely spaced layers of interconnect metal
- since Dass et al. does not provide for a thick layer of polyimide overlying interconnect traces, Dass et al. also does not provide for protection of the passivation film (by the thick layer of polyimide) that remains in place above the interconnecting traces
- the method that is provided by Dass et al. addresses problems that are experienced with a passive scrub cantilever needle probe card and the scrubbing process; these problems become particularly severe for smaller contact pad pitch of contact pads that are used for testing or probing of wafers; the contact pads that are therefore created by Dass et al. are wafer contact pads for testing purposes having a pitch of 80 microns
- the claimed invention addresses, in forming a thick layer of passivation (for improved protection of the underlying components) in the era of sub-micron devices and the therewith used closely spaced interconnect lines, the formation of keyholes between interconnect lines, which presents a concern since the thick layer of passivation (typically deposited by depositing two layers of passivation)

does not readily penetrate between narrowly spaced adjacent interconnect lines; for a typical process of etching (a passivation layer in order to expose a bonding pad) photoresist is used which, where keyholes are present, which is typically between adjacent interconnect traces, penetrates the keyholes; during subsequent high temperature processing, the photoresist deposits violently react to the high temperatures and "explodes" from the keyholes, causing significant disturbance to the process of device formation

- this latter phenomenon is to be prevented, the present claimed invention prevents this by using a thick layer of polyimide, whereby the polyimide readily penetrates any keyholes that may have formed between adjacent, closely spaced interconnect lines, and
- with the claimed invention, bond pads can be created without incurring processing damage caused by photoresist remnants that in conventional processing penetrates into keyholes between closely spaced interconnect lines.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 1-25 and 27-30 under 35 U.S.C 103(a) as being unpatentable over Dass et al. (US

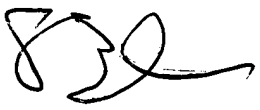
Patent 6,143,668) in view of Fu et al. (US Patent (5,807,787) be withdrawn.

Other Considerations

No new independent or dependent claims have been written as a result of this office action, no new charges are therefore incurred due to this office action.

It is requested that, should Examiner not find the claims to be allowable, to call the undersigned Attorney at the Examiner's convenience at 845-452-5863 in order to overcome any problems preventing allowance of the claims.

Respectfully submitted,



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